UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,451	10/24/2006	Kouji Miyauchi	P30330	1313

7055 7590 11/13/2008

GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER
BALDRIDGE, BENJAMIN M

ART UNIT	PAPER NUMBER
2831	

NOTIFICATION DATE	DELIVERY MODE
11/13/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

gbpatent@gbpatent.com
pto@gbpatent.com

Office Action Summary	Application No.	Applicant(s)	
	10/597,451	MIYAUCHI ET AL.	
	Examiner	Art Unit	
	Benjamin M. Baldridge	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3 November 2006, 19 October 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 12 are presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Figure 10: item number 6, mentioned in the specification, is missing from Figure 10.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

Page 2, paragraph 2: the expression "without a wealth of knowledge in the spectrum analyzer" is unclear. For the purposes of examination, it is assumed that the meaning is "without a high level of expertise in the use of a spectrum analyzer".

Page 15, 17: the term “WCDMA" is undefined in the specification. For the purposes of examination, “WCDMA” is assumed to mean “wideband code-division multiple access”.

Page 20 and elsewhere in the specification: Figure reference not found. References to item numbers on page 20 and elsewhere in the specification are not given a figure reference. For the purposes of examination, it is assumed that Figure 10 is the intended figure reference. For clarity, it is suggested that a general statement, such as "Like numbers denote like items in the various figures" be inserted after the brief description of the drawings, on page 7.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Takano et al. (US Patent 4,607,215, August 19, 1986, hereinafter referred to as Takano).

As to claim 1, Takano discloses a spectrum analyzer including:

A level adjuster that receives an output signal output from a device under test, adjusts a level of the output signal, and outputs the resulting output signal (Abstract, lines 1 – 3; Figure 1, items 1 – 2; note INPUT ATTENUATOR, and INPUT ATTENUATION SETTING CIRCUIT);

A characteristic measurer that receives the output signal output from said level adjuster and measures a characteristic of the device under test (Abstract, lines 1 - 2; Column 3, lines 24 - 26, 49 - 51; note explicit disclosure of a Spectrum Analyzer, an instrument that measures a characteristic of a device under test);

A level setter that sets a degree of an adjustment of the level of the output signal by said level adjuster so that a measurement error is minimum upon the measurement (Column 3, lines 1- 6, 49 -50; also Column 1, lines 5 – 14, disclosed as background of the invention, i.e. prior art).

As to claim 2, Takano discloses:

The measurement error is caused by said characteristic measurer and changes according to the level of the output signal supplied to said characteristic measurer (Column 1, lines 15 – 18, 27 – 32, disclosed as background of the invention; also Column 2, lines 47 – 52; note also Figure 1, items 1, 2, and 13, in which a control circuit in the spectrum analyzer (which is taken to be the "characteristic measurer") sets input attenuation).

As to claim 8, Takano discloses:

Said level setter discretely sets the degree of adjustment of the level of the output signal such that said level adjuster can adjust the level of the output signal such that the measurement error is minimum within a range equal to or lower than the level of the output signal which minimizes the measurement error (Abstract, lines 3 – 10; Column 2, lines 51 – 57; note A/D conversion of signals into the control circuit (item 13, Figure 2), which directly controls the input attenuation circuitry, Figure 1, items 1 and 2).

As to claim 10, the method disclosed in the instant claim is intrinsic to the device disclosed in claims 1 and 2, as discussed above, since the method steps will be met during the normal operation of the system stated above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 – 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takano in view of Fukui et al. (US Patent 6,229,316 B1, May 8, 2001, hereinafter referred to as Fukui).

As to claims 3 – 7 and 9, Takano discloses a device as discussed in paragraph 4 above. However, Takano fails to disclose:

A measurement error calculator that calculates the measurement error based on a signal purity, a distortion that increases the measurement error as the level of the output signal increases, and a noise that decreases the measurement error as the level of the output signal increases [claim 3]

The distortion is determined based on the IP3 of the measuring device [claim 4].

The noise is determined based on a noise level determined based on a frequency of the signal measured by said characteristic measurer [claim 5]

The noise is determined based on a modulation bandwidth of the output signal [claim 6]

The signal purity is determined based on a modulation bandwidth of the output signal [claim 7],

Said characteristic measurer comprises a digital processor which carries out digital processing; and said level setter sets the degree of the adjustment of the level of the output signal such that said level adjuster can adjust the level of the output signal such that the measurement error is minimum in a range which can be processed by the digital processor [claim 9]

Fukui discloses:

A measurement error calculator that calculates the measurement error (Figure 9, item S102) **based on a signal purity, a distortion that increases the measurement error as the level of the output signal increases, and a noise that decreases the measurement error as the level of the output signal increases** [claim 3] (Column 5, lines 40 – 48; note disclosure of carrier to noise ratio (C/N), which in this case is the signal purity, as defined in the specification; note also Column 5, lines 56 - 60, and Column 8, lines 16 - 27);

The distortion is determined based on the IP3 of the measuring device [claim 4] (Column 12, lines 42 – 48; Figure 2B, items 41 – 44; also Figure 4B, item 46a).

The noise is determined based on a noise level determined based on a frequency of the signal measured by said characteristic measurer [claim 5] (Figure 2A, item 38; note that the noise (in dBc) is shown as item 38; note also C/N ratio given as -53 dBc/Hertz; note also noise level shown at offset from the carrier at f_N).

The noise is determined based on a modulation bandwidth of the output signal [claim 6] (Figure 5A - note “MEASURING BAND WIDTH" shown on Figure 5).

The signal purity is determined based on a modulation bandwidth of the output signal [claim 7] (Figures 5A, 5B; also Column 5, lines 40 - 48; note that signal purity in this case is taken to be carrier to noise ratio, or C/N, as recited in the specification);

Said characteristic measurer comprises a digital processor which carries out digital processing; and said level setter sets the degree of the adjustment of the level of the output signal such that said level adjuster can adjust the level of the output signal such that the measurement error is minimum in a range which can be processed by the digital processor [claim 9] (Abstract, lines 17 – 23; Figure 1, item 13; note explicit disclosure of a CPU, clearly a digital processor, in the Abstract. Note also Takano, Column 3, lines 44 – 52 and Column 4, lines 54 – 61 of Takano).

Given the teaching of Fukui, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the device of Takano by employing well known or conventional features such as a measurement error calculator making calculations based on signal purity, distortion and noise, and incorporating a digital processor in the characteristic measurer, to carry out digital processing and adjust levels of output signals, as disclosed by Fukui, in order to automatically analyze signal purity, noise and intermodulation, and adjust input levels to a spectrum analyzer to minimize noise.

7. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takano in view of Muto et al. (US Patent 7,123,000 B2, October 17, 2006, hereinafter referred to as Muto).

As to claims 11 and 12, Takano discloses a device as discussed in paragraph 4 above.

Specifically, Takano discloses:

A level adjuster that receives an output signal output from a device under test, adjusts a level of the output signal, and outputs the resulting output signal; and a characteristic measurer that receives the output signal output from said level adjuster and measures a characteristic of the device under test [claims 11, 12] (Abstract, lines 1 – 3; Figure 1, items 1 – 2; note INPUT ATTENUATOR, and INPUT ATTENUATION SETTING CIRCUIT; also Abstract, lines 1 - 2; Column 3, lines 24 - 26, 49 - 51; note explicit disclosure of a Spectrum Analyzer, an instrument that measures a characteristic of a device under test);

Setting a degree of an adjustment of the level of the output signal by said level adjuster so that a measurement error is minimum upon the measurement [claims 11, 12] (Column 3, lines 1- 6, 49 -50; also Column 1, lines 5 – 14, disclosed as background of the invention, i.e. prior art).

(Note also that the methods disclosed in the instant claims are intrinsic to the device disclosed in claims 1 - 9, as discussed above, since the method steps will be met during the normal operation of the system stated above).

Takano fails to disclose:

A program of instructions for execution by the computer to perform a process of a measuring device [claim 11];

A computer-readable medium having a program of instructions for execution by the computer to perform a process of a measuring device [claim 12].

Muto discloses:

A program of instructions for execution by the computer to perform a process of a measuring device [claim 11] (Column 11, lines 3 – 10);

A computer-readable medium having a program of instructions for execution by the computer to perform a process of a measuring device [claim 12] (Column 11, lines 3 – 10).

Given the teaching of Muto, a person of ordinary skill in the art would have readily recognized the desirability and advantages of modifying the device of Takano by employing well known or conventional features such as a program of instructions for execution by a computer, and a computer readable medium to contain the instructions, as disclosed by Muto, in order to program a computer to operate a device to automatically analyze signal purity, noise and intermodulation, and adjust input levels to a spectrum analyzer to minimize noise.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin M. Baldridge whose telephone number is 571 270 1476. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571 272 2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Diego Gutierrez/
Supervisory Patent Examiner, Art Unit 2831

/Benjamin M Baldridge/
Examiner, Art Unit 2831